CLAIMS

1. A sensing circuit for a target memory cell, said sensing circuit comprising:

said target memory cell having a drain capable of being connected to a first node through a selection circuit during a read operation involving said target memory cell, said target memory cell drawing a target memory cell current when activated during said read operation;

a first transistor being connected across said first node and a second node;

a load being connected across said second node and a third node; and

a voltage boosting circuit being coupled to a supply voltage, said voltage boosting circuit supplying a voltage at said third node which is greater than said supply voltage.

2. The sensing circuit of claim 1 wherein a sense amp input voltage is generated at said second node during said read operation.

3. The sensing circuit of claim 1 wherein said target memory cell is capable of storing four charge levels.

4. The sensing circuit of claim 3 wherein said four charge levels comprises a first charge level drawing approximately 0 microamperes during said read operation, a second charge level drawing approximately 10 microamperes during said read operation, a third charge level drawing approximately 15 microamperes during said

read operation, and a fourth charge level drawing approximately 20 microamperes during said read operation.

5. The sensing circuit of claim 1 wherein said voltage boosting circuit comprises a charge pump driven by a two-phase clock.

6. The sensing circuit of claim 1 wherein a source of said target memory cell is coupled to a reference voltage, and a gate of said target memory cell is connected to a word line, said word line activating said target memory cell during said read operation.

7. The sensing circuit of claim 6, wherein said reference voltage is ground.

8. A multi-level charge memory device comprising:

a target memory cell having a drain capable of being connected to a first node through a selection circuit during a read operation involving said target memory cell, said target memory cell drawing a target memory cell current when activated during said read operation; and

a sensing circuit comprising a first transistor, a load, and a voltage boosting circuit, said first transistor being connected across said first node and a second node, said load being connected across said second node and a third node, said voltage boosting circuit being coupled to a supply voltage, said voltage boosting circuit supplying a voltage at said third node which is greater than said supply voltage.

9. The multi-level charge memory device of claim 8 wherein a sense amp input voltage is generated at said second node during said read operation.

10. The multi-level charge memory device of claim 8 wherein said target memory cell is capable of storing four charge levels.

11. The multi-level charge memory device of claim 10 wherein said four charge levels comprises a first charge level drawing approximately 0 microamperes during said read operation, a second charge level drawing approximately 10 microamperes during said read operation, a third charge level drawing approximately 15 microamperes during said read operation, and a fourth charge level drawing approximately 20 microamperes during said read operation.

12. The multi-level charge memory device of claim 8 wherein said voltage boosting circuit comprises a charge pump driven by a two-phase clock.

13. The multi-level charge memory device of claim 8 wherein a source of said target memory cell is coupled to a reference voltage, and a gate of said target memory cell is connected to a word line, said word line activating said target memory cell during said read operation.

14. The multi-level charge memory device of claim 13, wherein said reference voltage is ground.

15. A sensing circuit for a target memory cell, said target memory cell having a drain capable of being connected to a first node through a selection circuit during a read operation involving said target memory cell, said target memory cell drawing a target memory cell current when activated during said read operation, a first transistor being connected across said first node and a second node, said sensing circuit being characterized by:

a load being connected across said second node and a third node, a voltage boosting circuit being coupled to a supply voltage, said voltage boosting circuit supplying a voltage at said third node which is greater than said supply voltage.

16. The sensing circuit of claim 15 wherein a sense amp input voltage is generated at said second node during said read operation.

17. The sensing circuit of claim 15 wherein said target memory cell is capable of storing four charge levels.

18. The sensing circuit of claim 17 wherein said four charge levels comprises a first charge level drawing 0 approximately microamperes during said read operation, a second charge level drawing approximately 10 microamperes during said read

operation, a third charge level drawing approximately 15 microamperes during said read operation, and a fourth charge level drawing approximately 20 microamperes during said read operation.

19. The sensing circuit of claim 15 wherein said voltage boosting circuit comprises a charge pump driven by a two-phase clock.

20. The sensing circuit of claim 15 wherein a source of said target memory cell is coupled to a reference voltage, and a gate of said target memory cell is connected to a word line, said word line activating said target memory cell during said read operation.